its upper surface is below the upper surface. Fulford teaches that the dielectric material is either formed level with the surface of the substrate or formed below the surface of the substrate. Therefore, among other reasons, Fulford does not disclose the claimed invention, which contains in part that the first compound is partially removed from the trench such that the upper surface of the compound is below the surface of the substrate. Further, after a fair reading of Fulford, one with ordinary skill in the art of electronic components and electronic component assembly would not be able to comprehend that the dielectric material is added to the trench and then partially removed such that the upper surface of the compound is below the surface of the substrate, given that Fulford never discusses or claims this option. The Examiner points to Column 7, lines 4-50 to support her contention that Fulford anticipates claim 12 of the present application; however, in column 7, lines 25-28, Fulford clearly discloses that the "etchback technique is performed to remove the upper surface of the dielectric material to a level approximately commensurate with the upper surface of the substrate. 50." The Merriam Webster dictionary defines "commensurate" as "equal in measure or extent". Figures 5-8 and 10 are also cited as Examples as to how Fulford, Jr. teach that the dielectric material is added to the trench and then etched back, but the Figures taken in context with the specification do not lead to that conclusion and in the Applicant's opinion, do not anticipate the present application. Therefore, Fulford does not anticipate the present application, because Fulford does not contemplate adding the dielectric material to the trench and then partially removing it such that the upper surface of the compound is below the surface of the substrate.

In addition, Fulford does not teach all of the claimed elements of the present application. "Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Assocs. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing *Soundscriber Corp. v. United States*, 360 F.2d 954, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)) Further, the prior art reference must disclose each element of the claimed invention "**arranged as in the claim**". *Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)(citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)). Fulford does not teach a method for forming a shallow trench isolation structure where the first compound is partially removed from the trench such that an upper surface of the compound is below the surface of

the substrate. Based on this argument, along with others such as that discussed above, Fulford does not anticipate claim 12 of the present application because Fulford is lacking and/or missing at least one specific feature or method recitation found in the present application, and in claim 12. Claim 12 is therefore allowable as not being anticipated by Fulford. Further, Fulford does not anticipate claims 14 and 17-19 of the present application by virtue of their dependency on claim 12.

Claims 12 and 13 are herein rejected under 35 USC §102(e) as being anticipated by Gardner et al. (US 6,194,283). The Applicant respectfully disagrees.

Claim 12 recites "A method of forming a shallow trench isolation structure, comprising: forming a trench in a substrate having a surface, and **depositing a first compound into the trench using spin-on deposition**; partially removing the first compound from the trench such that an upper surface of the compound is below the surface of the substrate; and depositing a second compound onto the substrate surface and onto the upper surface of the first compound by chemical vapor deposition." (emphasis added)

Gardner et al. (Gardner) teaches a method of forming an isolation trench in a semiconductor substrate that is substantially free of voids, wherein an oxide layer is formed in the trench and all layers and materials are applied by vapor deposition. Therefore, among other reasons, Gardner does not disclose the claimed invention, which contains in part that the first compound is deposited by spin-on deposition. Further, after a fair reading of Gardner, one with ordinary skill in the art of electronic components and electronic component assembly would not be able to comprehend that the materials or layers could be deposited by any other method other than vapor deposition methods, given that Gardner never discusses or claims this option. The Examiner contends that Gardner using "spin on deposition" is "inherent" (see Paper No. 9, page 3, Point 4); however, the Applicant strongly disagrees, especially given the fact that Gardner only discloses CVD and PVD application processes and states in Column 3, lines 35-45 that the isolation dielectric is a "CVD oxide".

In addition, Gardner does not teach all of the claimed elements of the present application.

"Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Assocs. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing *Soundscriber Corp. v. United States*, 360 F.2d 954, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)) Further, the prior art reference must disclose each element of the claimed invention "**arranged as in the claim**". *Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)(citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)). Gardner does not teach a method of depositing a first compound into the trench using spin-on deposition. Based on this argument, along with others such as that discussed above, Gardner does not anticipate claim 12 of the present application because Gardner is lacking and/or missing at least one specific feature or method recitation found in the present application, and in claim 12. Claim 12 is therefore allowable as not being anticipated by Gardner. Further, Gardner does not anticipate claim 13 of the present application by virtue of its dependency on independent claim 12.

35 USC §103

Claims 15-16 are herein rejected under 35 USC §103(a) as being unpatentable over Gardner et al. (US 6,194,283) in view of Koyanagi (US 6,191,002). The Applicant respectfully disagrees.

Claim 12 recites "A method of forming a shallow trench isolation structure, comprising: forming a trench in a substrate having a surface, and **depositing a first compound into the trench using spin-on deposition**; partially removing the first compound from the trench such that an upper surface of the compound is below the surface of the substrate; and depositing a second compound onto the substrate surface and onto the upper surface of the first compound by chemical vapor deposition." (emphasis added)

Gardner et al. (Gardner) teaches a method of forming an isolation trench in a semiconductor substrate that is substantially free of voids, wherein an oxide layer is formed in the trench and all layers and materials are applied by vapor deposition. Therefore, among other reasons, Gardner does not disclose, teach or suggest the claimed invention, which contains in part that the first compound is

deposited by spin-on deposition. Further, after a fair reading of Gardner, one with ordinary skill in the art of electronic components and electronic component assembly would not be able to comprehend that the materials or layers could be deposited by any other method other than vapor deposition methods, given that Gardner never discusses or claims this option. The Examiner contends that Gardner using "spin on deposition" is "inherent" (see Paper No. 9, page 3, Point 4); however, the Applicant strongly disagrees, especially given the fact that Gardner only discloses CVD and PVD application processes and states in Column 3, lines 35-45 that the isolation dielectric is a "CVD oxide". And based on this argument, among others, claim 12 of the present application is not obvious in view of Gardner. Further, claims 15 and 16 are not obvious in view of Gardner by virtue of their dependency on claim 12.

Koyanagi teaches a method of forming a trench isolation structure wherein the oxide film of the silicon covering the main surface of the substrate is selectively removed leaving a part of the oxide film above the surface of the substrate that is used as an isolation dielectric of a trench isolation structure (see Abstract and Figures). Therefore, among other reasons, Koyanagi does not disclose, teach or suggest the claimed invention, which contains in part that the first compound is partially removed such that the upper surface of the compound is below the surface of the substrate. Further, after a fair reading of Koyanagi, one with ordinary skill in the art of electronic components and electronic component assembly would not be able to comprehend that the materials or layers could be removed in such a way that the dielectric or oxide material is above the surface of the substrate, given that Koyanagi never discusses or claims this option. And based on this argument, among others, claim 12 of the present application is not obvious in view of Koyanagi. Further, claims 15 and 16 are not obvious in view of Koyanagi by virtue of their dependency on claim 12.

Finally, with regard to the present rejection, there is no motivation or suggestion to combine or modify the Gardner reference in view of Koyanagi, especially given the fact that Gardner does not teach, suggest or disclose spin-on deposition of materials and given the fact that Koyanagi does not teach, suggest or disclose removing the oxide material in such a way where the surface of the oxide material is below the surface of the substrate. Based on this argument, among others including those discussed above, claim 12 is allowable as patentable over Gardner in view of Koyanagi. Further, claims 15 and 16 are allowable as patentable over Gardner in view of Koyanagi by virtue of their

dependency on independent claim 12.

Claim 22 (canceled and now part of independent claim 20) is herein rejected under 35 USC §103(a) as being unpatentable over Endisch et al. (US 6,140,254) in view of Kurosawa et al (US 6,011,123). The Applicant respectfully disagrees.

The Applicant has previously submitted a Declaration Under 37 USC § 1.132 that removes Endisch as a prior art reference related to the 103 rejection. As mentioned in the Declaration:

- ✓ Both the above-referenced application and US 6,140,254 were originally commonly owned by AlliedSignal Inc. at the time the later invention was made.
- ✓ Both the above-referenced application and US 6,140,254 have been subsequently assigned to Honeywell International Inc.
- ✓ Both the above-referenced application and US 6,140,254 share a common inventor: Denis H. Endisch.

The Applicant furthermore refers the Examiner to MPEP §718: Affidavit or Declaration to Disqualify Commonly Owned Patent as Prior Art, 37 CFR 1.130. As stated, "When any claim of an application...is rejected under 35 USC 103 on a US patent or US patent application publication which is not prior art under 35 USC 102(b), and the inventions defined by the claims in the application...and by the claims in the patent or published application are not identical but are not patentably distinct, and the inventions are owned by the same party, the applicant...may disqualify the patent as prior art...by submission of: a) a terminal disclaimer, and b) an oath or declaration stating that the application and patent are currently owned by the same party, and that the inventor named in the application is the prior inventor under 35 USC 104." Furthermore, when an application claims an invention which is not patentably distinct from an invention claimed in a commonly owned

patent with **the same or different inventive entity**, a double patenting rejection will be made in the application. (emphasis added). In this case, a terminal disclaimer filed in accordance with §1.321(c) shall be filed.

In this instance, given that the Applicant has shown that the present application and the Endisch reference are commonly owned and by different inventive entities , the proper rejection is a double patenting rejection which can be readily overcome by filing a terminal disclaimer in accordance with 37 CFR 1.321(c). Therefore, in order to expedite this matter, the applicant has attached herein a Terminal Disclaimer under 37 CFR 1.321(c). The Applicant has also herein attached a Declaration under 1.130(a).

Therefore, Endisch cannot properly be considered a prior art reference by the Examiner, as based on the previous showing that the Endisch reference and the current application are commonly owned at the time the later invention was made. Further, independent claim 20 is allowable as being patentable over Endisch. The Applicant respectfully invites the Examiner to contact the undersigned Attorney-of-Record, if this issue remains unresolved by this Response.

Since the Examiner is citing Kurosawa et al as a secondary reference – dependent on the primary Endisch reference, and since the Endisch reference can properly be removed as a prior art reference according to the attached terminal disclaimer and declaration, the Kurosawa reference cannot stand alone as a primary reference to preclude patentability of claim 20. Therefore, claim 20 is allowable in view of the Endisch reference.

REQUEST FOR ALLOWANCE

Claims 1 2-20 a re p ending i n t his a pplication. The applicants request allowance of all pending claims.

Respectfully submitted,

Rutan & Tucker, LLP

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By: /Sandra Thompson/

Sandra P. Thompson, PhD, Esq.
Reg. No. 46,264
E-mail: sthompson@rutan.com
Direct Line: 714-641-3468

Attorneys for Applicant(s)
611 Anton Boulevard, Fourteenth Floor
Costa Mesa, CA 92626-1998
Tel: (714) 641-5100
Fax: (714) 546-9035

MARKED UP COPY OF THE CURRENT/PENDING CLAIMS

12. A method of forming a shallow trench isolation structure, comprising:

forming a trench in a substrate having a surface, and depositing a first compound into the trench using spin-on deposition;

partially removing the first compound from the trench such that an upper surface of the compound is below the surface of the substrate; and

depositing a second compound onto the substrate surface and onto the upper surface of the first compound by chemical vapor deposition.

13. The method of claim 12 further comprising planarizing the isolation structure such that the surface of the substrate and an upper surface of the second compound are substantially coplanar.

14. The method of claim 12 wherein the substrate surface and the trench further comprise a thermal oxide coat.

15. The method of claim 13 wherein the trench has an aspect ratio (depth/width) of no less than 5.

16. The method of claim 12 further comprising curing the first compound to form an oxide.

17. The method of claim 12 wherein the step of partially removing comprises a process selected from the group consisting of a spin-rinse process, a wet etch process, and a dry etch process.

18. The method of claim 12 wherein the first compound is formed from at least one compound selected from the group consisting of methylsilsesquioxane, hydrogensilsesquioxane, methylhydridosilsesquioxane, silicate, and perhydrosilazane.

19. The method of claim 12 wherein the second compound is formed from tetraethylorthosilicate or silane.

20. (Amended) A method of removing a spin-on compound, comprising:

spin-depositing a spin-on compound on a surface of a substrate, wherein the spin-on compound comprises silicon, wherein the first solvent comprises propyl acetate, and wherein the second solvent comprises ethyl lactate; and

spin-rinsing the spin-on compound with a solvent mixture, wherein the solvent mixture comprises a first solvent that dissolves the spin-on compound, and a second solvent that is inert to the spin-on compound.

21. Cancel.

22. Cancel.

23. Cancel.

CLEAN COPY OF THE CURRENT/PENDING CLAIMS

12. A method of forming a shallow trench isolation structure, comprising:

forming a trench in a substrate having a surface, and depositing a first compound into the trench using spin-on deposition;

partially removing the first compound from the trench such that an upper surface of the compound is below the surface of the substrate; and

depositing a second compound onto the substrate surface and onto the upper surface of the first compound by chemical vapor deposition.

13. The method of claim 12 further comprising planarizing the isolation structure such that the surface of the substrate and an upper surface of the second compound are substantially coplanar.

14. The method of claim 12 wherein the substrate surface and the trench further comprise a thermal oxide coat.

15. The method of claim 13 wherein the trench has an aspect ratio (depth/width) of no less than 5.

16. The method of claim 12 further comprising curing the first compound to form an oxide.

17. The method of claim 12 wherein the step of partially removing comprises a process selected from the group consisting of a spin-rinse process, a wet etch process, and a dry etch process.

18. The method of claim 12 wherein the first compound is formed from at least one compound selected from the group consisting of methylsilsesquioxane, hydrogensilsesquioxane, methylhydridosilsesquioxane, silicate, and perhydrosilazane.

19. The method of claim 12 wherein the second compound is formed from tetraethylorthosilicate or silane.

20. (Amended) A method of removing a spin-on compound, comprising:

spin-depositing a spin-on compound on a surface of a substrate, wherein the spin-on compound comprises silicon, wherein the first solvent comprises propyl acetate, and wherein the second solvent comprises ethyl lactate; and

spin-rinsing the spin-on compound with a solvent mixture, wherein the solvent mixture comprises a first solvent that dissolves the spin-on compound, and a second solvent that is inert to the spin-on compound.

21. Cancel.

22. Cancel.

23. Cancel.